Abstract of the Disclosure

The method for manufacturing an FeRAM capacitor with a merged top electrode plate line (MTP) structure is employed to prevent a detrimental impact on the FeRAM and to secure a reliable FeRAM device. The method includes steps of: preparing an active matrix obtained by a predetermined process; forming a first conductive layer, a dielectric layer and a second conductive layer on the active matrix in sequence; forming a hard mask on the second conductive layer; patterning the second conductive layer, the dielectric layer and the first conductive layer by using the hard mask, thereby forming a vertical capacitor stack, a width of the capacitor stack being larger than that of the storage node contact; forming a second ILD embracing the capacitor stack; planarizing the second ILD till the top face of the hard mask is exposed; removing the hard mask to form an opening above the top electrode; and forming a plate line of which a width is larger than that of the capacitor stack.